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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No. BU9-97-224B
Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS

and invented by:

Philip S. Honsinger, Andrew D. Huber, Debra K. Korejwa, William J. Livingstone, Jeannie H. Panner, Erich C. Schanzenback, Douglas W. Stout, Steven H. Voldman and Paul S. Zuchowski

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☒ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: **09/015,819**

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below
2. ☒ Specification having **23** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☒ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

UTILITY PATENT APPLICATION TRANSMITTAL
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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 8
   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration
   a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☐ Certificate of Mailing
   ☐ First Class ☐ Express Mail *(Specify Label No.):* **HAND DELIVERED**

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Docket No. BU9-97-224B
Total Pages in this Submission

Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra		Rate	Fee
Total Claims	20	- 20 =	0	x	$18.00	$0.00
Indep. Claims	5	- 3 =	2	x	$80.00	$160.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$710.00
OTHER FEE *(specify purpose)*						$0.00
					TOTAL FILING FEE	$870.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. **09-0456** as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of **$870.00** as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Kevin C Reif
Signature

Dated: **October 4, 2000**

Kevin A. Reif
Reg. No. 36,381

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cc:

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Philip S. Honsinger et al.
Filed: Concurrently herewith

Divisional Application of:

Serial No. 09/015,819 Group Art Unit: 2814
Filed: January 29, 1998 Examiner: H. Pham

For: METHOD OF AUTOMATED DESIGN
AND CHECKING FOR ESD ROBUSTNESS

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Prior to examination on the merits, please amendment above identified patent application as follows:

IN THE SPECIFICATION:

On page 1, line 3, beneath the title, insert the following:

--This application is a divisional of U.S. application Serial No. 09/015,819 filed on January 29, 1998, now abandoned.

IN THE CLAIMS:

Please cancel claims 1-6 without prejudice or disclaimer

Please add the following claims:

--21. A computer readable medium comprising instructions for a computer implemented chip design method, said method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints; and

e) checking said wired integrated circuit.

22. The computer readable medium comprising instructions as recited claim 21, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

23. The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including a connection to power rail or to a power return rail.

24. The computer readable medium comprising instructions as recited in claim 22, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including an ESD

protect device.

25. The computer readable medium comprising instructions as recited in claim 22, wherein the generating step (d) comprises the step of:

i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

26. The computer readable medium comprising instructions as recited in claim 25, wherein the checking step (e) comprises checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints.--

REMARKS

Claims 1-6 have been canceled. Claims 7-26 are presented for examination on the merits. Claims 21-26 are *Beauregard*-type claims (*In re Beauregard*, 35 USPQ2d 1383, CAFC, 1995) and have been newly added to further define the scope of Applicant's invention. In particular, these claims substantially parrot claims 7-12 except that the preamble has been modified to recite that the claimed method can be tangibly stored in machine readable form for execution by a computer. Examination on the merits is respectfully requested.

Please charge any deficiencies in fees and credit any overpayment of fees to Assignee's Deposit Account No. 09-0456.

Respectfully submitted,

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APPLICATION FOR UNITED STATES LETTERS PATENT

Applicants: Philip S. Honsinger, Andrew D. Huber, Debra K. Korejwa, William J. Livingstone, Jeannie H. Panner, Erich C. Schanzenbach, Douglas W. Stout, Steven H. Voldman and Paul S. Zuchowski

For: METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS

Docket No.: BU9-97-224B

METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS

DESCRIPTION

RELATED APPLICATION

The present invention is related to U.S. Patent Application No.08/_____ (Attorney Docket No. BU9-97-176) entitled "Method of Automated ESD Protection Level Verification" to Bass et al., filed coincident herewith and assigned to the assignee of the present application.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to integrated circuit design, checking and verification and more particularly to methods of integrated circuit placement, wiring, checking and verification for electrostatic discharge robustness.

Background Description

Electrostatic discharge (ESD) protect devices, connected to integrated circuit (IC) chip's input/output (I/O) pads to protect circuits on the chip from ESD damage are well known in the art. ESD damage may result from ESD

between any two chip pads. Typically, prior art ESD devices were designed and located based on well understood requirements of the particular circuit or, cell, and the physical characteristics of the chip technology and the ESD protect device. Thus, for a single power supply chip, the ESD device may have been, merely, a pair of reverse biased diodes, each connected between the supply or its return line (ground) and an IC chip signal pad.

The characteristics of (i.e., the level of protection afforded by) these prior art ESD protect devices were determined by the pad to ESD device wiring and the circuit attached to the pad. The design objective is to insure that the ESD device turns on before the circuit or wiring to the circuit fails. Thus, wiring between the pad and the ESD device must be wide enough to transfer the charge to the device without failing during the transfer.

However, even with a wire that is wide enough, if its resistance is too high, due to its length, the combination of the resistance and wiring/ESD device capacitance filters the charge provided to the ESD device, reducing its effectiveness. Under some circumstances, the wiring resistance in the I/O net wiring may act as a voltage divider. If the pad to device resistance is high enough, the voltage dropped across the divider resistance may prevent the device from ever turning on.

As long as what is typically referred to as the chip image (the template for an IC defining pad locations and chip size) is well defined, the above problems can be adequately addressed fairly simply by design. Thus, in Figure 1 which shows an example of a prior art standard chip image 50, the chip has well defined circumferentially located I/O cells 52 and ESD protect devices (not shown) predefined power busses connected to an external connection pad 54. Circumferentially located signal pads 56 are connected through the ESD protect devices to I/O cells 52.

Typical electrical characteristics considered in designing an ESD network are: type of wiring metal (aluminum or copper, etc.), as well as wire and via (inter metal-metal layer connections) dimensions, i.e., widths, lengths, thicknesses and contact sizes. Thus, for a standard image 50 by design, each individual I/O cell may have a fixed, well defined internal resistance associated with it, thereby assuring the ratio of fixed wire resistance to internal cell resistance.

Advances in IC technology have increased circuit density, increasing the number of circuits on a single chip. The increase in the number of circuits has led to a corresponding increase in the number of pads for off chip connections, i.e., for chip inputs/outputs (I/Os) and for supplying power and ground to the chip according to what is well known in the art as Rent's Rule. Consequently, to take full advantage of this increased IC chip gate count and complexity and to provide more locations for chip pad connections, standard chip images such as chip image 50 in Figure 1 cannot be used.

Further, ESD protection is more complex on a multiple supply chip. Besides providing a supply path and a ground or return discharge path, paths must be provided from each pad 54 to each additional power supply line and each additional return line. Each signal pad 56 must be connected through an ESD protect device to each supply and each return. An ESD device for such a typical multi-supply IC chip may be nothing more than a string of diodes. Other chip characteristics, such as a power sequencing requirement, may further complicate the device.

So, for example, on a 2-supply chip, even a circuit in an I/O cell 52 connected to a single supply still requires a an ESD protection path through a device connected between its connecting pad and the unused (by that I/O circuit) supply. While this requirement may be met without difficulty for a

standard image chip 50 by including protect devices periodically spaced around the chip's perimeter; it makes wiring an already complex chip even more difficult for a non-standard image chip.

Further complicating this, is that with the increased I/O count requirement on state of the art non-standard image IC chips, I/O cell placement is not restricted to the chip's periphery, the normal location for ESD devices. Instead, with a non-standard area array footprint, wires connecting I/O circuits to the chip pads are routed individually, either automatically by a design system or, interactively by a designer. Further, power busses are not as well defined and do not provide the extra protection from the added capacitance found on prior art standard images 50.

Thus, there is a need for integrated circuit chips with pad array interconnections having robust ESD protection and for a system and method for designing IC chips with robust ESD protection and verifying the IC chip design.

SUMMARY OF THE INVENTION

It is therefore a purpose of the present invention to improve integrated circuit chip ESD protection.

It is another purpose of the present invention to allow free form I/O cell placement on integrated circuit chip without impairing chip ESD protection.

It is yet another purpose of the present invention to verify ESD protection on integrated chips.

The present invention is a integrated circuit (IC) chip with ESD robustness and the system and method of designing and verifying the IC chip.

Minimum wire width and maximum resistance constraints are applied to each of the chip's I/O ports. These constraints are propagated to the design. Array pads are wired to I/O cells located on the chip. Unused or floating pads may be tied to a supply or ground line, either directly or through an ESD protect device. A multi-supply protect device (ESDxx) coupled between pairs of supplies and ground or return lines is inserted. Thus, wiring is such that wires and vias to ESD protect devices are wider than signal wires. All chip pads have adequate ESD protection. The I/O power bus has robust ESD protection. The design may then be verified.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 shows a prior art standard image footprint;

Figure 2 shows an example of a chip designed according to the preferred embodiment method of the present invention;

Figure 3 is a flow chart of the preferred embodiment method of ASIC design and checking;

Figure 4 is a flow chart of the preferred embodiment method of ASIC design for I/O circuit instance to pad connection for ESD robustness;

Figure 5, which is a flow chart of a second preferred embodiment method that insures ESD robustness for unused external pads and for I/O power distribution;

Figure 6 is an example of an instruction for connecting an unused external pad to ground;

Figure 7 is an example of an instruction for connecting an appropriate supply voltage type to an I/O circuit having ESD devices;

Figure 8 is a flow chart of a preferred embodiment method for insuring ESD robustness on multiple power supply chips; and

Figure 9 shows I/O circuit instances on a multi-supply IC that are grouped together physically in a configuration with an ESDxx circuit instance embedded in the group.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to Figure 2, which shows a pad array chip 60 designed according to the preferred embodiment method to provide robust I/O and power connections. I/O circuits instances 62, 64 may be located throughout the chip 60 and are connected to pads 66, 68. Pads 68 are located over core circuit areas 70. Nets 72 between I/O cell instances 64 and pads 68 and nets 74 between I/O cell instances 62 and pads 66 having been formed according to the preferred embodiment design method have robust ESD protection.

According to the preferred embodiment method, each I/O instance 62, 64 includes an ESD protect device and connection between the ESD device therein and the cell's active circuitry. Thus, the preferred embodiment method is intended for IC chips 60 where power distribution is a mesh of wires on several conductive (metal) levels. The mesh is modifiable to allow the addition of large circuit blocks, sometimes referred to as megacells or large memory bocks. Each power supply is represented as a single network, e.g., there is a single VDD net with all circuits requiring VDD connected to the VDD net. External pad locations are predefined and have predefined

functions, i.e., predefined as power supply or signal for inclusion in pre-designed packaging.

Three sources of technology library information are included with each preferred embodiment application specific IC (ASIC) design. These three sources include a technology file, an IC image information file, and individual circuit files for each circuit in the technology library.

The technology file contains information that is constant for all IC images and all circuit elements. The technology file contains predefined allowable wire widths and RC information for these widths. Also, the technology file includes a lookup table for obtaining information concerning minimum wire width and maximum resistance constraints.

The image files contain information about a default power grid, location and function of the external pads, allowable I/O circuit instance placement rules, instructions for dealing with any external pads left unused, instructions for modifying the base power grid around large circuit elements, and placement requirements for an ESDxx circuit.

Power bus information is included as pattern specifications, used by a power bus router to insert power bussing into the IC design as required. Included in this power bus pattern specification is a series of instructions that allow the power bus router to enhance power distribution in the vicinity of I/O circuits. This ensures that I/O circuit power route wires are wider than a minimum width and have line resistance below a maximum resistance sufficient to provide a minimum level of ESD protection, i.e., that the ESD network is robust enough to handle ESD events within a specified range.

The unused pad specification lists a wire width to be used when routing connections between unused external pads and the nearest power

buses. This ensures that each unused external pad is connected to the power distribution net with a connection robust enough to handle an ESD event.

If necessary, a pointer for each connection point, commonly referred to as a "pin", may be included in each circuit's circuit file. These pointers would reference information in the technology file regarding maximum resistance and minimum wire width constraints for any net connected to the pin associated with the pointer.

Although the preferred embodiment of the present invention was developed to function on the IBM® ChipBench design tool, the present invention maybe adapted for any suitable design tool.

Figure 3 represents the preferred embodiment IC physical design method to ensure ESD robustness. In the preferred method, the chip is designed using circuit and image abstracts without device-level checking. All ESD ground rules are checked in I/O circuits prior to chip design, prior to being used on the chip.

Thus, in step 80, the chip net list and the technology data needed for physical design and checking are read into the tool. Also, the chip physical design database is initialized, which includes supplying a base chip image and power grid to the tool. The chip's logic pins may be only partially assigned to external pads.

In step 82, the chip floorplan is determined using both interactive manual tools and automatic tools. At this stage, chip logic pins are assigned to chip pads, objects are placed in the image, global routes are created, and the design is analyzed. After this step 82, the completed floorplan has megacells and I/Os placed; all external pads assigned; approximate placement set for the logic; the power grid; and, the placed design has been analyzed to determine

whether it is wireable, meets timing requirements and satisfies technology constraints.

Next, in step 84, logic placement details are finalized. This may include minor logic placement perturbation or full timing-driven re-placement, including clock tree (clock distribution) optimization to minimize skew and latency and meet previously defined objectives, as well as optimizing scan nets.

Next, in step 86, the power routing is finalized by customizing the base power grid for the chip. This step may also include truncating the power grid at power rings of megacells and, enhancing the base power grid in areas where required, e.g. near I/O circuit instances. In step 88, signals are routed. Wide wires, wires wider than a minimum width, may be routed in advance of the rest of the design nets or, concurrently (on the fly) as minimum width nets are routed.

Finally, in step 90, the design is checked at the abstract level. All design rules (logical, physical/electrical, test design rules) are checked against technology requirements. The design should be correct by construction at the device level.

I/O cells and the IC in general may be checked at the device level, as described in related to U.S. Patent Application No. 08/_____ (Attorney Docket No. BU9-97-176) entitled "Method of Automated ESD Protection Level Verification" to Bass et al., filed coincident herewith and assigned to the assignee of the present application and incorporated herein by reference. After checking, the resulting ASIC may be manufactured using well known techniques.

Figure 4 is a flow chart of the preferred embodiment method of ASIC design for I/O signal ESD robustness. First, in step 100, technology data that

includes minimum wire width constraints on I/O cell pin to external signal pad connections is provided.

The tool reads these minimum wire width constraints from the technology data. This first constraint, wire width, is technology dependent and is the minimum value required both to ensure acceptable ESD protection and to meet any wire electromigration requirements. This first constraint, which may vary layer by layer, is specified as a wire width for each routing layer and as a minimum via number and minimum via area for each interlevel via layer.

Next, in step 102, maximum resistance constraints are read from the technology data. The technology data also includes maximum pin resistance allowed between the I/O cell pin and an external signal pad. These resistance constraints ensure acceptable circuit ESD protection.

The constraints are applied individually to each net as follows: 1) All pins on a net are inspected to determine worst-case constraints for the net; and, 2) The determined worst-case constraints are applied to the whole net. So, for example for determining the minimum wire width constraint for any particular net, the worst-case constraint for the net is the maximum of the set of minimum wire width constraints found on all the pins of the net. For the maximum resistance constraint, the worst-case constraint is the smallest maximum resistance constraints on all of the pins of the net.

So, in step 104, at the beginning of physical design, the design system propagates I/O cell pin constraints in the technology data to the ASIC's net constraints, where they are applied by the design tool. Thus, every net that includes a connection between an I/O cell instance pin and an external signal pad has a minimum wire width constraint and a maximum resistance

constraint. Optionally, these net constraints may be manually overridden with more stringent constraints by the designer.

The next step 106 is chip physical design, as described hereinabove with respect to Figure 3 taking into account net constraints in floorplanning, placement, and signal routing tools. The floorplanner uses the constraints during chip pad assignment to I/O circuit instance pins.

Net constraints are included in the cost functions that drive the decisions made by the placement tools. If after placement, no route exists for a net, the tools estimate the net resistance using the net's minimum wire width constraint and a Steiner route. The net wire width constraints are followed by the signal routing tools.

In step 108, the maximum resistance I/O pin constraints in the technology data are applied to each design net connected to an external pad by the checking tool. Each net's total resistance is compared to the maximum resistance net constraint. This check may be done prior to routing a net using an estimated route for the net. Similarly, the I/O pin minimum wire width constraints in the technology data are applied to each net connected to an external pad by the checking tool. A smallest wire width is determined for each net and compared to the minimum wire width constraint.

Any I/O nets failing the checks may be fixed by changing the pad assignment of the I/O pin, by changing the location of the I/O cell, by widening the failing wire to increase allowable wire length, or by rerouting the net.

At physical design completion, the checking program verifies that all nets satisfy the technology constraints. Preferably, the checking program is run earlier to minimize fixes and overall design time. Thus, having identified

any failures or a constraint violation, the design may be altered to correct the violation.

Figure 5, which is a flow chart of a second preferred embodiment method, that insures ESD robustness for unused external pads and for I/O power distribution and may be combined with the first preferred embodiment. Unused external pads are not identifiable, nor is the location of I/O circuits containing ESD protect devices known until the IC is being personalized. However, the unused pads must be connected to ground and the I/O circuit ESD protect devices must be connected to an appropriate voltage type.

In the second preferred embodiment method, technology dependent instructions are provided in step 110 to a power route program, each instruction describing one pattern of power metal to be generated. Figure ~~6~~ is an example of an instruction for connecting an unused external pad to ground. Figure 7 is an example of an instruction for connecting an appropriate supply voltage type to an I/O circuit with ESD devices, or an ESDxx cell.

Each instruction includes a section characterizing the connection being made and a section with the metal parameter necessary for creating a robust connection. As each instruction is read a pattern is created. Patterns are order dependent. Subsequent patterns may rely on shapes created by earlier patterns.

Thus, for a given instruction, the power route program, in step 112, by identifies objects to be connected. One instruction can select many objects. Each selected object satisfies a number of criteria set forth in the instruction. The selected objects must be of a specified type. Object types include power service terminals (pins), power routes, and unused external pads.

Further, selected objects must belong to a circuit in a specified library circuit group or belong to the IC. Library circuit groups are established as

part of the technology. A circuit can belong to one or more library groups. The selected object must occur within a specified region relative to the circuit which owns the object and upon any one layer of a specified set of layers.

Each object is associated with one of two ends or the middle of the connection. Ultimately, the end of a connection is associated with a single object. Any number of objects may be associated with the middle of a connection. The selected objects forming the connection must be located within a rectangle. The middle objects occur within the rectangle and the two end objects occur at the ends of the rectangle.

The objects selected by reading one instruction are not necessarily associated with a single connection. Objects are divided into connections based upon the selected middle objects. The middle objects must be approximately aligned along a specified axis and must occur within a specified proximity of each other. Any middle objects satisfying these constraints are associated with one connection. The creation of multiple connections may be necessary in order for all middle objects to be included in a connection. End objects must be within a specified proximity of a middle object and must be aligned with the middle objects along the given axis. The closest such end object is associated with the connection of middle objects. If no end object satisfies the above constraint, a connection is created without an end object.

At the end of the identification phase for an instruction, a set of connections has been identified. Each connection includes at least one middle object. The end objects may not always be present. However, normally there is an end object, a sequence of middle objects and a second end object. Further, the set of objects forming the connection are approximately aligned along a specified axis.

In step 114, each connection is routed as a continuous metal shape connecting shapes of objects. Routing avoids obstacles according to constraints specified in the instruction creating the power routing connection. Each power route metal shape is constrained to occur within a guide box derived from a parameter in the instruction and the location of objects in the connection.

In step 116 the technology data is inspected for remaining instructions. If any instructions remain to be processed, then return to step 110. Otherwise proceed to step 118. As a result unused external pads are connected to an ESD network, e.g., ground and every I/O circuit instance power pin has a robust connection to an appropriate power supply.

Finally, to avoid having errors inadvertently introduced in the ASIC design, in step 118 a checking program verifies the design. The checking program independently reads the technology power routing instructions and the chip design. The power routes are traced for the connections to be made. Routes are compared to the technology instructions (e.g., width by metal layer). If design errors indicate that a connection fails to meet minimum technology criteria, an error report is generated and the design must be corrected.

So, in the example of Figure 6, an instruction (PowerPattern) results in metal connecting an unused external pad (MiddleType) of the chip (MiddleOwner) to a ground power (End1Type, ConnectNet) of the chip (End1Owner). Only unused pads on layer M5 (MiddleLayer) anywhere within the chip are considered. Only ground power located on layer M5 (End1Layer) of the chip are considered. The ground power must be within 2000 microns (End1Proximity) of the unused pad. The metal that is created is associated with the ground net (ConnectNet). The ground net is located on layer M4

(ConnectLayer) and has a width of 16.3 microns (ConnectWidth). Its route is allowed to vary 58.1 microns (ConnectSwath) about a vertical line (ConnectAxis) in order to avoid obstacles. Vias are added between the metal on M4 and the pad on M5 and the power on M5 as needed.

In the example of Figure 7, an instruction (PowerPattern) is one of several that result in metal connecting possibly several VDD power pins (MiddleType, ConnectNet) of the cells in the library cell group ESD (MiddleOwner) to a VDD power (End1Type, End2Type, ConnectNet) of the chip (End1Owner, End2Owner). Only power pins on layer M2 (MiddleLayer) within the a specified region (MiddleStart, MiddleEnd) of a cell above are considered. Only VDD pins located on layer M5 (End1Layer, End2Layer) of the chip are considered. There may be several VDD power pins in the same connection provided they are positioned along a vertical axis (MiddleAxis) and are within 180 microns (MiddleProximity) of another. A VDD power must be at either end of the pins and within 2000 microns (End1Proximity, End2Proximity) of a pin. The metal that is created is associated with the VDD net (ConnectNet). It is located on layer M4 (ConnectLayer) and has a width of 16.3 Microns (ConnectWidth). Its route Must be perfectly straight (ConnectSwath) along a vertical line (ConnectAxis). Another instruction is used to create metal on M3 and vias are used as needed to finalize the connection.

An alternative embodiment to ensure ESD protection for unused signal pads is to connect such a pad to an instance of a special library cell containing an active ESD device or a direct connection to a power supply within the cell. In this embodiment, the netlist would contain the circuit instance, which would be placed with the other I/O circuit instance placement. The net would be routed by the signal router and the robustness of the connection would be

checked with the other signal routes. This alternative embodiment would follow the method of Figure 4.

Figure 8 is a flow chart of a third preferred embodiment method for ensuring ESD robustness on multiple power supply chips. In the preferred embodiment, a robust ESD mesh exists everywhere on the IC for VDD1. The VDD2 supply is routed only to I/O circuit instances requiring that supply. On multiple power supply ICs (e.g., an IC with VDD1 and VDD2 power supplies) a multi-supply protect device, referred to herein as an ESDxx device must be included. Instances of the ESDxx device must be in a sufficient ratio and proximity to I/O circuit instances utilizing VDD2 to ensure ESD robustness. By ensuring the proximity to the ESDxx device to I/O circuit instances, a low resistance power bus network is guaranteed. The I/O circuit instances themselves may also have placement constraints for various reasons.

First, in step 120, I/O and ESDxx cells are identified and read from technology library data along with the placement constraints for each cell type. So, for example as represented in Figure 9, there may be a requirement that I/Os requiring VDD2, e.g. 130, be grouped together physically in certain configurations that guarantee robust power routing. Still another requirement might be to provide an ESDxx cell, e.g. 132, for each such physical group 134, with the ESDxx circuit 132 instance embedded in or, abutted to the group 134. The example in Figure 9 shows a 2×4 group 134 of I/O circuit instances 130 wherein the ESDxx cell 132 is embedded.

Alternatively, I/O cells may not be required to be grouped together, but may be allowed to be placed freely. All I/O circuit instances would be connected to multiple supplies through the ESDxx devices. In this case, some number of ESDxx cells may be required for I/O cells within a particular

region, based on the power supply network's physical and electrical configurations.

So, next, in step 122, the chip floorplan is determined and all I/O circuit instances are placed according to technology placement constraints. Then, in step 124, the I/O circuit instance placements are analyzed to determine the number of ESDxx circuit instances that are required. The required number are added to the netlist and placed according to the technology constraints. Finally in step 126, I/O and ESDxx cell placement are checked by an independent checking program which checks each cell placement against the technology constraints to determine whether the design meets these minimum requirements.

It is understood that an IC may include two or more power supplies and, further may include one or more ground or return lines with appropriate modification. Such a chip would also include appropriately designed ESDxx cells placed in appropriate locations.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

We claim:

1. An integrated circuit chip comprising:

an array of pads, said pads including signal I/O, power and power return pads;

a plurality of I/O cells each being connected to one of said I/O pads by I/O signal wiring in one or more wiring layers; and

a plurality of ESD protection devices, each of said plurality of ESD protection devices being connected to one of said array of pads by a metal line, said metal line meeting an ESD width constraint and having a resistance below an ESD resistance constraint.

2. The integrated circuit chip of Claim 1, wherein the plurality of ESD protection devices comprises:

an ESD protect device in each of said plurality of I/O cells connected between an I/O circuit in said I/O cell and one of said I/O signal pads.

3. The integrated circuit of claim 2 wherein each said ESD protect device is further connected to power rails and power return rails connected to said circuit.

4. The integrated circuit chip of claim 3, wherein the plurality of ESD protection devices comprises:

an ESDxx cell connected between power rails and power return rails for at least two different power supplies.

5. The integrated circuit chip of claim 4 further comprising:

a plurality of ESDxx cells, each of said plurality of ESDxx cells being associated with a group of I/O cells.

6. The integrated circuit chip of claim 5 further comprising:

a plurality of said I/O signal lines being designated as unused, said unused I/O signal lines being connected to one of said power or power return rails.

7. A chip design method comprising the steps of:

a) retrieving a wire width constraint from technology data for an I/O cell;

b) retrieving a maximum resistance constraint from said technology data for said I/O cell;

c) propagating said wiring width constraint and said maximum resistance constraint to net design data for said chip;

d) generating said chip, connections between said I/O cell and an associated pad being constrained by said propagated constraints; and,

e) checking said wired integrated circuit.

8. The method of claim 7, wherein a plurality of I/O cells are wired and further comprising before the checking step (e), repeating steps (a) - (d) for each of said plurality of I/O cells.

9. The method of claim 8, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including a connection to power rail or to a power return rail.

10. The method of claim 8, further comprising before the checking step (e), the step of:

d1) wiring any unused chip pads to a cell including an ESD protect device.

11. The method of claim 8, wherein the generating step (d) comprises the step of:

i) placing each of said I/O cells based on said propagated wire width and maximum resistance constraints; and

ii) routing a connection between each said placed I/O cell and its said associated pad, each said routed connection meeting said propagated wire width and maximum resistance constraints.

12. The method of claim 11, wherein the checking step (e) comprises checking connections made in said generating step (d) against propagated wire width and maximum resistance constraints.

13. A chip design method comprising the steps of:

a) retrieving a power route pattern instruction;

b) identifying power and power return connections;

c) routing each said power and each said power return connection, each said routed connection meeting wire width and maximum resistance constraints in said retrieved power route pattern instruction; and

d) checking said wired integrated circuit.

14. The method of claim 13, wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a power rail or to a power return rail.

15. The method of claim 13, wherein the routing step (c) includes identifying any unused chip pads and wiring said unused pad to a cell including an ESD protect device.

16. The method of claim 13, wherein the routing step (c) includes the steps of:

i) providing an ESDxx cell; and

ii) connecting said ESDxx cell between power rails and power return rails for at least two different power supplies.

17. A chip design method comprising the steps of:

a) retrieving I/O and ESDxx cell identifications and placement constraints;

b) providing a plurality of ESDxx cells for placement;

c) placing each of said plurality of ESDxx cells with a group of I/O cells;

d) connecting each said placed ESDxx cell between power rails and power return rails for at least two different power supplies; and,

e) checking said wired integrated circuit.

18. A system for integrated circuit chip design comprising:

means for retrieving net constraints from technology data;

means for placing a plurality of I/O cells; and

means for connecting each of said placed I/O cells to I/O cells to an I/O pad according to said retrieved net constraints.

19. The system of claim 18, wherein said retrieved constrains include power bussing constraints, said system further comprising:

means for routing power and power return connections according to said power bussing constraints.

20. The system of claim 18, further comprising:

means for grouping I/O cells; and

means for placing an ESDxx cell with each group of I/O cells.

METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS

ABSTRACT OF THE INVENTION

A integrated circuit (IC) chip with ESD robustness and the system and method of wiring the IC chip. Minimum wire width and maximum resistance constraints are applied to each of the chip's I/O ports. These constraints are propagated to the design. Array pads are wired to I/O cells located on the chip. Unused or floating pads may be tied to a power supply or ground line, either directly or through an electrostatic discharge (ESD) protect device. A multi-supply protect device (ESDxx) coupled between pairs of supplies and ground or to return lines is also included. Thus, wiring is such that wires and vias to ESD protect devices are wide enough to provide adequate ESD protection. Robust ESD protection is afforded all chip pads. The design may then be verified.

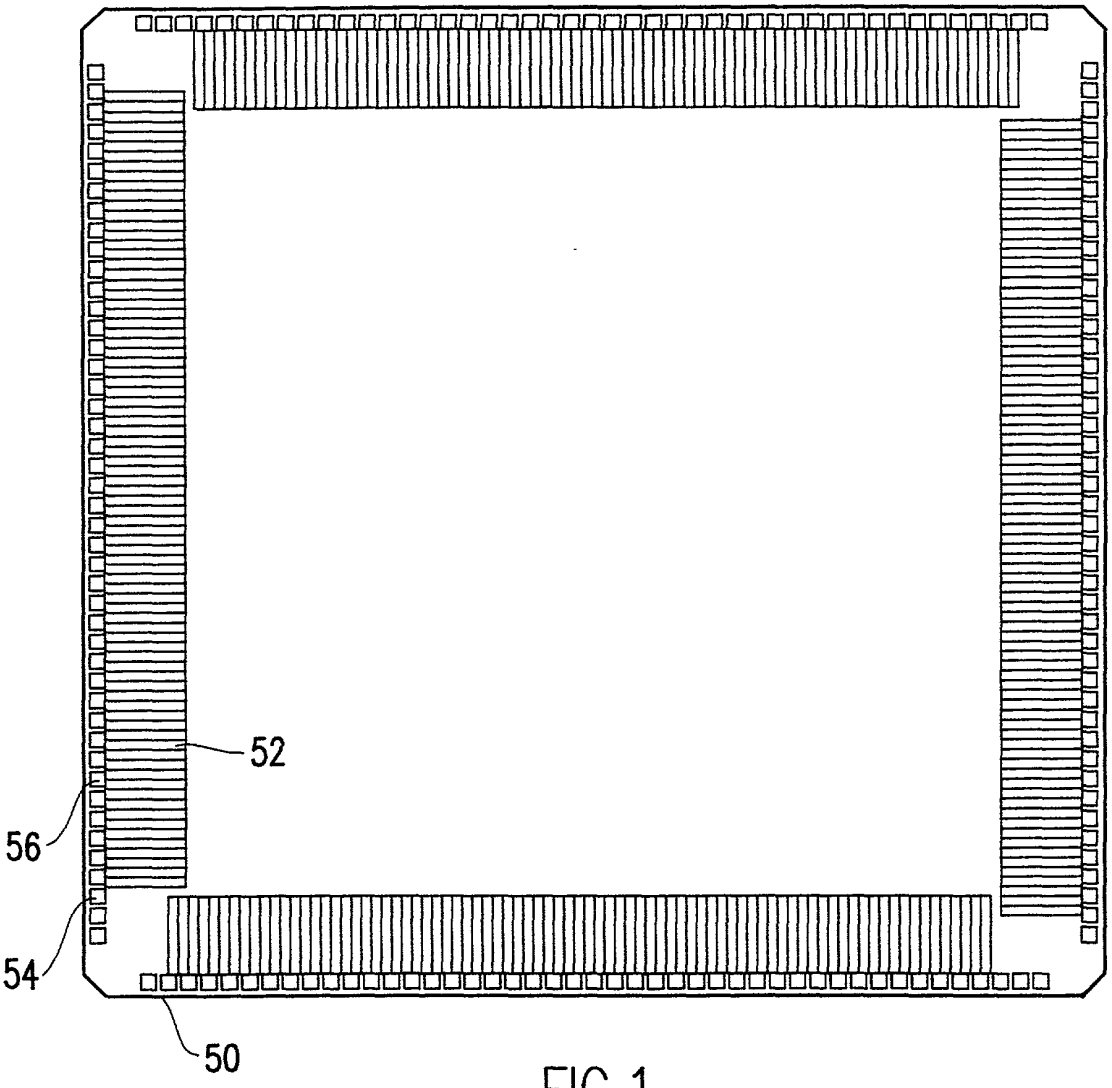

FIG. 1
PRIOR ART

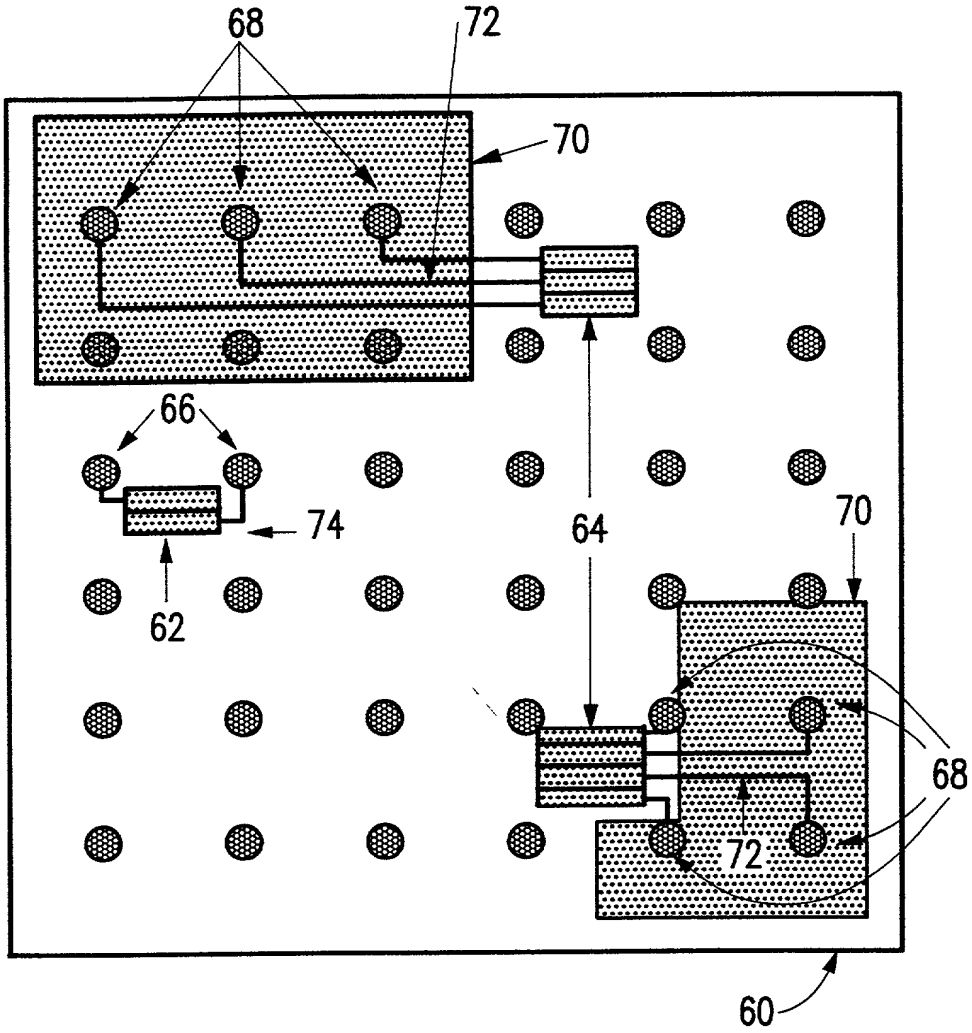

FIG.2

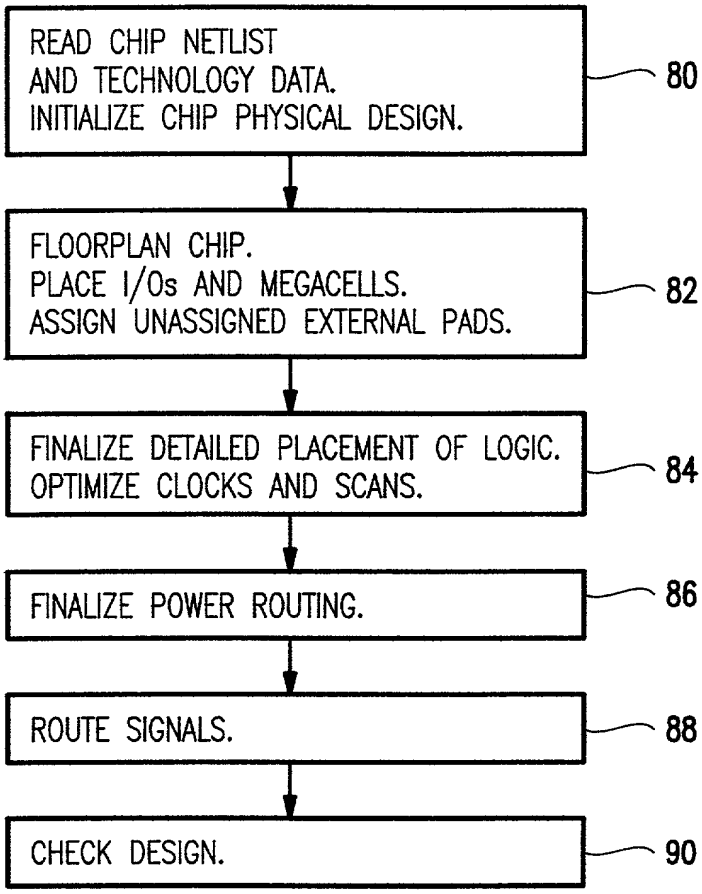
READ CHIP NETLIST
AND TECHNOLOGY DATA.
INITIALIZE CHIP PHYSICAL DESIGN.
80
FLOORPLAN CHIP.
PLACE I/Os AND MEGACELLS.
ASSIGN UNASSIGNED EXTERNAL PADS.
82
FINALIZE DETAILED PLACEMENT OF LOGIC.
OPTIMIZE CLOCKS AND SCANS.
84
FINALIZE POWER ROUTING.
86
ROUTE SIGNALS.
88
CHECK DESIGN.
90

FIG.3

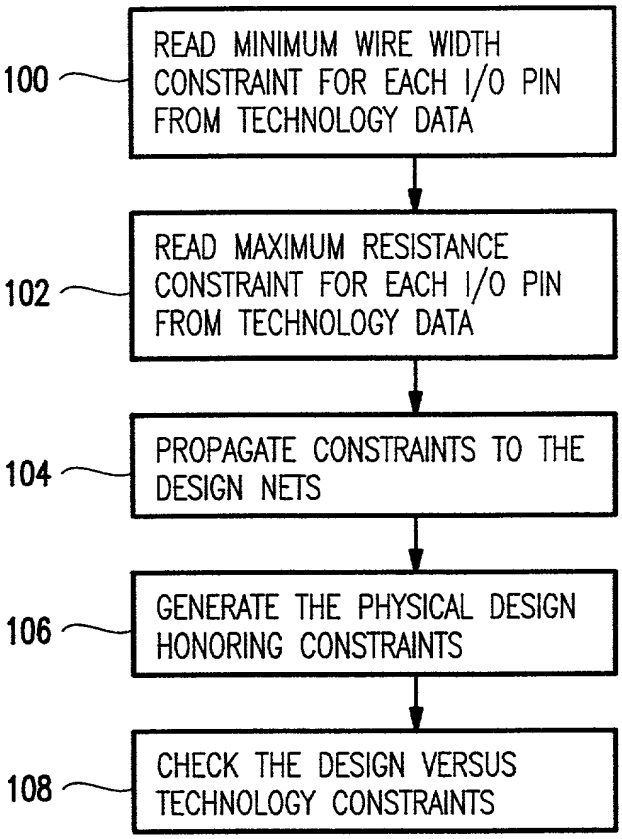
100
READ MINIMUM WIRE WIDTH CONSTRAINT FOR EACH I/O PIN FROM TECHNOLOGY DATA
102
READ MAXIMUM RESISTANCE CONSTRAINT FOR EACH I/O PIN FROM TECHNOLOGY DATA
104
PROPAGATE CONSTRAINTS TO THE DESIGN NETS
106
GENERATE THE PHYSICAL DESIGN HONORING CONSTRAINTS
108
CHECK THE DESIGN VERSUS TECHNOLOGY CONSTRAINTS

FIG.4

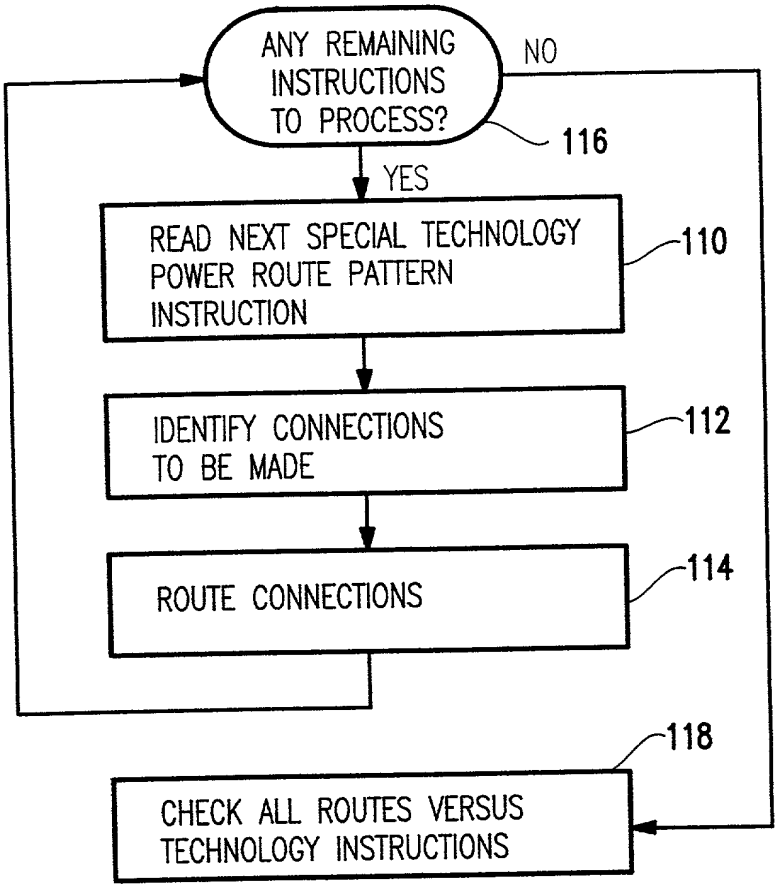
ANY REMAINING INSTRUCTIONS TO PROCESS?
NO
116
YES
READ NEXT SPECIAL TECHNOLOGY POWER ROUTE PATTERN INSTRUCTION
110
IDENTIFY CONNECTIONS TO BE MADE
112
ROUTE CONNECTIONS
114
118
CHECK ALL ROUTES VERSUS TECHNOLOGY INSTRUCTIONS

FIG.5

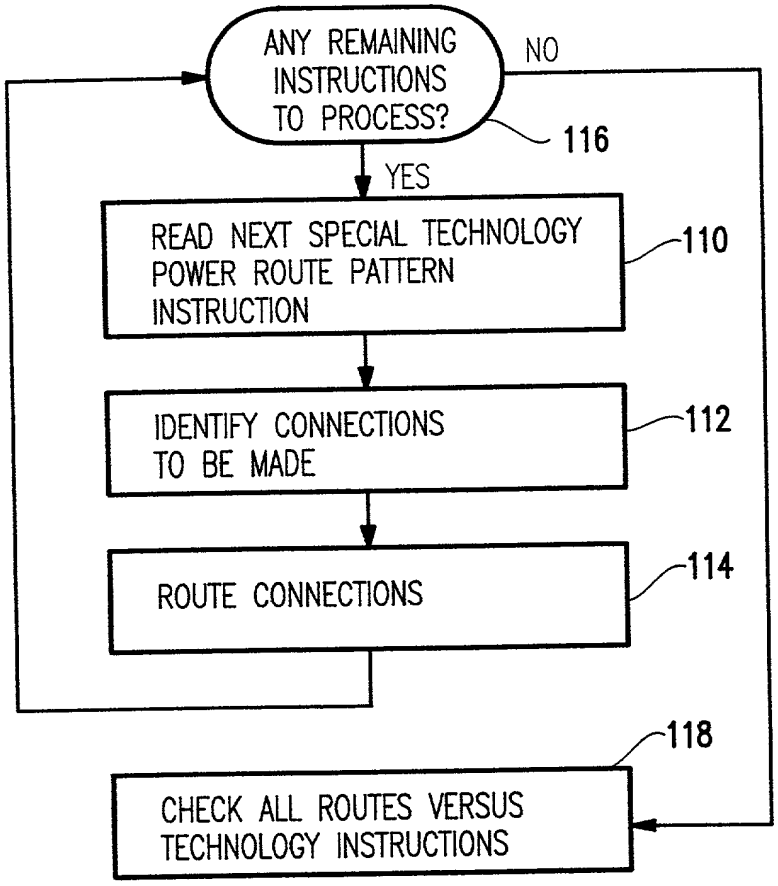
ANY REMAINING INSTRUCTIONS TO PROCESS?
NO
116
YES
READ NEXT SPECIAL TECHNOLOGY POWER ROUTE PATTERN INSTRUCTION
110
IDENTIFY CONNECTIONS TO BE MADE
112
ROUTE CONNECTIONS
114
118
CHECK ALL ROUTES VERSUS TECHNOLOGY INSTRUCTIONS

FIG.5

```
PowerPattern.GND_M4_UNUSED = {

    MiddleType      = UNUSEDPIN
    MiddleOwner     = CHIP
    MiddleLayer     = M5

    End1Type        = POWER
    End1Owner       = CHIP
    EndiLayer       = M5
    EndiProximity   = 2000  MICRON

    ConnectNet      = GND
    ConnectLayer    = M4
    ConnectWidt     = 16.3  MICRON
    ConnectSwath    = 58.1  MICRON
    ConnectAxis     = AXISVER
    }
```

FIG.6

```
PowerPattern.VDD_M4_ESD = {

        MiddleType      = PIN
        MiddleOwner     = ESD
        MiddleLayer     = M2
        MiddleStart     = (70.0 MICRON, 0.0 MICRON, LOWER_LEFT)
        MiddleEnd       = ( 0.0 MICRON, 0.0 MICRON, UPPER_RIGHT)
        MiddleAxis      = AXISVER
        Middleproximity = 180 MICRON


        End1Type        = POWER
        End1Owner       = CHIP
        End1Layer       = M5
        End1Proximity   = 2000 MICRON

        End2Type        = POWER
        End2Owner       = CHIP
        End2Layer       = M5
        End2proximity   = 2000 MICRON

        ConnectNet      = VDD
        ConnectLayer    = M4
        ConnectAxis     = AXISVER
        ConnectWidth    = 16.3 MICRON
        ConnectSwath    = 0 MICRON
        }
```

FIG.7

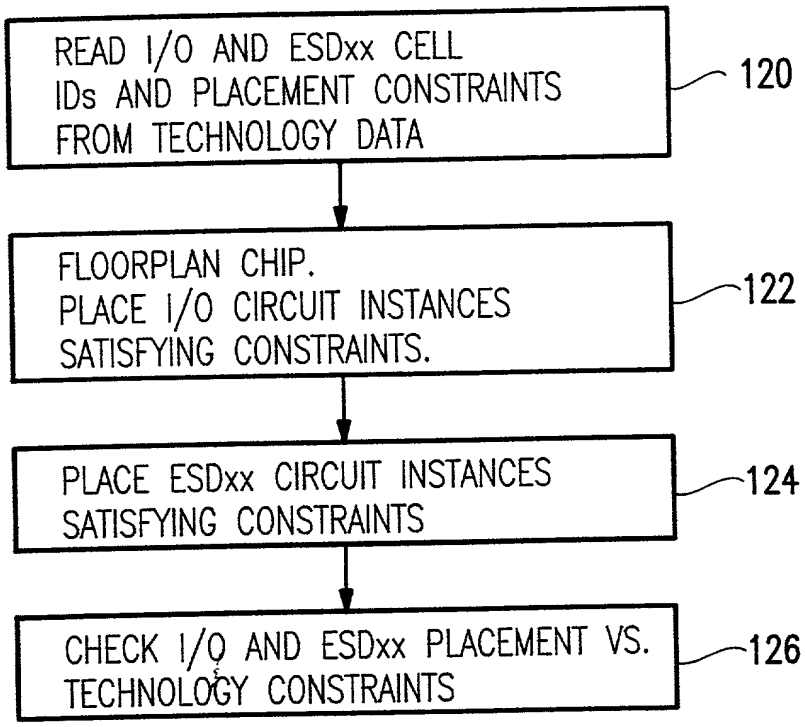
READ I/O AND ESDxx CELL IDs AND PLACEMENT CONSTRAINTS FROM TECHNOLOGY DATA
120
FLOORPLAN CHIP. PLACE I/O CIRCUIT INSTANCES SATISFYING CONSTRAINTS.
122
PLACE ESDxx CIRCUIT INSTANCES SATISFYING CONSTRAINTS
124
CHECK I/O AND ESDxx PLACEMENT VS. TECHNOLOGY CONSTRAINTS
126

FIG.8

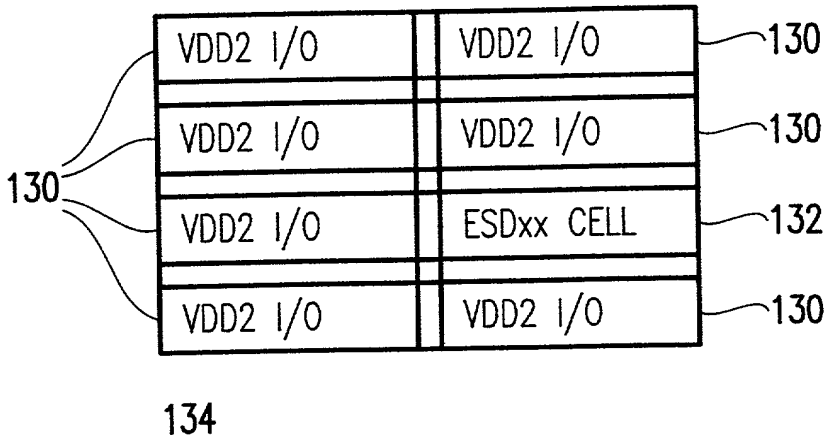
VDD2 I/O
VDD2 I/O
130
VDD2 I/O
VDD2 I/O
130
130
VDD2 I/O
ESDxx CELL
132
VDD2 I/O
VDD2 I/O
130
134

FIG.9

(JOINT INVENTOR)
Atty. Docket No.: BUS-97-224

Declaration and Power of Attorney for Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: ***METHOD OF AUTOMATED DESIGN AND CHECKING FOR ESD ROBUSTNESS*** the specification of which (check one)

[X] is attached hereto.

[ ] was filed on _____ as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed
NONE			

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status
NONE		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Floyd E. Anderson, (Reg. No. 33,825), Mark F. Chadurjian, (Reg. No. 30,739), John E. Hoel, (Reg. No. 26,279), Christopher A. Hughes, (Reg. No. 26,914), Richard M. Kotulak, (Reg. No. 27,712), James M. Leas (Reg. No. 34,372), Edward A. Pennington, (Reg. No. 32,588), Joseph C. Redmond, Jr., (Reg. No. 18,573), William D. Saba, (Reg. No. 27,465), Eugene I. Shkurko, (Reg. No. 36,678), Robert A. Walsh, (Reg. No. 26,516), Howard J. Walter, Jr., (Reg. No. 24,832), C. Lamont Whitham, (Reg. No. 22,424), Marshall M. Curtis, (Reg. No. 33,138), and Michael E. Whitham, (Reg. No. 32,635); as attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. All correspondence should be directed to Whitham, Curtis & Whitham, Reston International Center, 11800 Sunrise Valley Dr., Suite 900, Reston, Virginia 20191. Telephone calls should be directed to Whitham, Curtis, Whitham & McGinn at (703) 391-2510.

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